Please replace the specifications that describe the former Figure 11 with the specification that describe the new Figure 10, 11 and 12.

Figure 2A, 2B, 4 and 5 were amendment as suggested by the Examiner.

Figures 10, 11 and 12 have been added and the drawings are renumbered.

Please replace Figure 2A in the Front page.

IN THE CLAIMS:

The Applicant has amended claims 1-12 as suggested by the Examiner. The applicant added few new claims for a better overall understanding of the invention. Therefore, please replace claims 1-12 with the revised claims 1-15 (where claims 1, 10 and 11 were deleted). Attached hereto is a copy of the claims showing the amendments with underlining and brackets. Also attached is a clean copy of claims, as they stand after this amendment.

As the Examiner recommended, claims 2 and 12 became independent claims with claims 3- 9 depending from claim 2 and claims 13-14 depending from claim 12. Please enter the amended claims in the above mentioned application.

At the same time, the Applicant believes that revised claims explicitly reciting the specific arrangement of elements of the cell C(k) in two variants (claim 2 and claim 12, respectively) provide a different claiming for a better understanding of the invention.

The cell C(k) of claim 2 includes three memory words and it is used to calculate the logical value of a product term which is a constituent of one or several sum-of-product logical equations which define a combinational or a sequential target circuit to be implemented in a dynamically reconfigurable VLSI device. Having the cell C(k) of claim 2 as basic element, the same product term which is a constituent of several sum-of-product equations is implemented only once in the reconfigurable VLSI device.

In claim 12, the modified cell C(k) has two memory words and is used to calculate the logical value of a product term which is a constituent of one and only one sum-of-product logical equation from a group of equations which define a combinational or a sequential target circuit to be implemented in a dynamically reconfigurable VLSI

device. Having the modified cell C(k) of claim 12 as basic element, the same product term which is a constituent of several sum-of-product equations is implemented several times in the reconfigurable VLSI device, once for each equation where it is a component.

In all claims, the term "logical summing elements" has been replaced with the same mining term "OR gates" and the term "equivalence gates" has been replaced with the same mining term "XNOR gates".

The method of claim 15 is exemplary for defining an implementation of a target circuit defined by sum-of-products logical equations in a reconfigurable VLSI device containing the inventive cell C(k).

Consideration of new claims 13-15 would be much appreciated. The Applicant understands that protecting the two solution of the cell C(k) in independent claims may be practical as the cells are distributed in the layers of the VLSI devices. On the other hand, claim 15 are a reflection of the steps for dynamically reconfiguration of a VLSI devices using the inventive cell C(k), to implement combinational and sequential target circuits. Such a presentation helps the reader to easily understand the invention and complies with 35 USC 112, 2nd paragraph.

Clean copy of the claims

1 (Canceled)

2 (Currently amended) A dynamically reconfigurable VLSI device for implementing in hardware any multiple outputs combinational target circuit having the output functions expressed in logical sum-of-product equations with a maximum of m inputs, a maximum of r outputs and a maximum of n product terms p(k), comprising:

a register with m bits for storing the input variables;

n cells, a cell C(k) for determining the logical value of a product term p(k) of said equations for given inputs;

a block of r OR gates, each one with n inputs, associated with said cells C(k) for receiving the logical value of product terms p(k) and outputting the r bits of output functions;

wherein said cell C(k) comprises:

a storage area for storing the information that characterizes a product term, named mask word, product word and function word;

first logic level means for receiving said m inputs and said mask word to produce a first intermediate result, which identify the input variables that form a product term;

second logic level means for comparing the said product term with said first intermediate result to produce a second intermediate result concerning a product term;

third logic level means for receiving said second intermediate result to produce the logical value of the product term; and

forth logic level means for transferring said function word to r outputs, according to said logical value of said product term p(k), and subsequently to be OR-ed with function words of other product terms.

3 (Currently amended) A dynamically reconfigurable VLSI device as in claim **2**, wherein said storage area of a cell C(k) comprises two m-bit registers and one r-bit register.

4 (Currently amended) A dynamically reconfigurable VLSI device as in claim **2**, wherein said first logic level of a cell C(k) comprises m*(2-bit) AND gates, each one for receiving a respective bit of said m input variables and of said mask word to produce said first intermediate result.

5 (Currently amended) A dynamically reconfigurable VLSI device as in claim **2**, wherein said second logic level of a cell C(k) comprises m*(2-bit) XNOR gates, each one for receiving a respective bit of said first intermediate result and of said product word to produce a bit of said second intermediate result.

6 (Currently amended) A dynamically reconfigurable VLSI device as in claim **2**, wherein said third logic level of a cell C(k) comprises one m-bit AND gate to produce a logical value which is the value of the product term.

7 (Currently amended) A dynamically reconfigurable VLSI device as in claim **2**, wherein said forth logic level of a cell C(k) comprises m*(2-bit) AND gates for transferring said function word to outputs, considering the logical value of said product term p(k).

8 (Currently amended) A dynamically reconfigurable VLSI device for implementing in hardware any target synchronous sequential circuit with clock input only and outputs taken from the state register, further comprising:

a state register with s bits for storing the state variables;

a combinational part implemented as described in claim **2,** expressing the next state functions in logical sum-of-product equations, with a maximum of s inputs and outputs, and a maximum of n product terms p(k); and

a feedback connection to establish the next state.

9 (Currently amended) A dynamically reconfigurable VLSI device for implementing in hardware any synchronous sequential circuit with clock input and data inputs, further comprising:

a register with m bits for storing the input variables;

a state register with s bits for storing the state variables;

a first combinational part which is implemented as described in claim **2,** expressing the next state functions in logical sum-of-product equations with a maximum of m+s inputs, a maximum of s outputs, and a maximum of n1 product terms p(k);

a second combinational part which is implemented as described in claim **2,** expressing the output functions in logical sum-of-product equations, with a maximum of s inputs, a maximum of r outputs, and a maximum of n2 product terms p(k); and

a feedback connection to establish the next state.

10 (Canceled)

11 (Canceled)

12 (Currently amended) A dynamically reconfigurable VLSI device for implementing in hardware any multiple-output combinational target circuit defined by a group of logical sum-of-product equations, with maximum m inputs, maximum r outputs and a maximum of q product terms in each equation, having a register with m bits for storing the input variables and for each single sum-of-products logical equations, considered as an independent equation, further comprising:

q modified cells, a modified cell C(k) for determining the logical value of a product term p(k) of said independent equation, for given inputs;

a single OR gate associated with said q modified cell C(k) for receiving the logical value of product terms p(k) to provide a single output for said independent equation;

wherein said modified cell C(k) comprises:

a storage area formed by two m-bit registers for storing the information that characterizes a product term, named mask word and product word;

first logic level that comprises m*(2-bit) AND gates, each one for receiving a respective bit of said inputs and of said mask word to produce a respective bit of first intermediate result, which identify the input variables that form a product term;

second logic level that comprises m*(2-bit) XNOR gates, each one for receiving a respective bit of said product word and said first intermediate result to produce a second intermediate result concerning a product term; and

third logic level that comprises one m-bit AND gate for receiving the m bits of said second intermediate result to produce a logical value which is the value of the product term.

13 (New) A dynamically reconfigurable VLSI device for implementing in hardware any target synchronous sequential circuit with clock input only and outputs taken from the state register, further comprising:

a state register with s bits for storing the state variables;

a combinational part implemented as described in claim **12**, expressing the next state functions in logical sum-of-product equations with a maximum of s inputs and outputs, and a maximum of q product terms p(k) in each considered sum-of-product independent equation; and

a feedback connection to establish the next state.

14 (New) A dynamically reconfigurable VLSI for implementing in hardware any synchronous sequential circuit with clock input and data inputs, further comprising:

a register with m bits for storing the input variables;

a state register with s bits for storing the state variables;

a first combinational part which is implemented as described in claim **12**, expressing the next state functions in logical sum-of-product equations with a maximum of m+s inputs, a maximum of s outputs, and a maximum of q1 product terms p(k) in each considered independent sum-of-product equation;

a second combinational part which is implemented as described in claim **12**, expressing the output functions in logical sum-of-product equations with a maximum of s inputs, a maximum of r outputs, and a maximum of q2 product terms p(k) in each considered independent sum-of-product equation; and

a feedback connection to establish the next state.

15 (New) A method for implementing in a dynamically reconfigurable VLSI device a target circuit selected from multiple-output combinational circuits and from synchronous sequential circuits, defined by groups of sum-of-product logical equations, in limits imposed by the parameters number of inputs, number of outputs and number of product terms, the method comprising the steps of:

inputting a request to reconfigure said VLSI device to said target circuit;

identifying the VLSI device to be configured, considering its internal structure of cell C(k) as described in any one of claims **2** or **12**;

generating memory words uniquely defining each product term p(k) of said sum-of-products logical equations; and

implementing the target circuit by storing each said memory words into a corresponding register of a cell C(k) as defined in any one of claims **2** or **12**.